

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hieu Van TRAN et al.

Serial No.: 09/929,542

Group Art Unit: 2824

Filed: August 13, 2001

Examiner: Dinh, Son T.

Title: **ARRAY ARCHITECTURE AND OPERATING METHODS FOR DIGITAL
MULTILEVEL NONVOLATILE MEMORY INTEGRATED CIRCUIT SYSTEM**Certificate of Transmission by Facsimile

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Sir:

In response to the Office Action mailed June 4, 2003, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 17 of this paper.

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U.S. Serial No.: 09/929,542

Filing Date: August 13, 2001

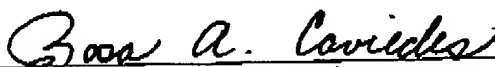
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Enclosed is:

1. Amendment.

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